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10/721,178	11/26/2003	Shih-Lien L. Lu	INTEL-0034	6618

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EXAMINER	
KIM, DANIEL Y	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 01/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/721,178	LU ET AL.	
	Examiner	Art Unit	
	Daniel Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20,25 and 26* is/are rejected.

7)☒ Claim(s) *21-24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, lines 1-4 disclose "a memory comprising a plurality of memory arrays wherein each memory array has a memory array architecture similar to an apparatus architecture of an apparatus coupled to the plurality of memory arrays". This language does not allow one of ordinary skill in the art to determine the scope of the claimed invention. For purposes of this action, this limitation will be interpreted as the claimed invention comprising an apparatus coupled to a plurality of memory arrays.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-2, 5-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Iwamura et al (US Patent No. 6,467,004).

For claim 1, Iwamura discloses a memory comprising an apparatus coupled to the plurality of memory arrays (a pipelined semiconductor device, such as a pipelined data processing device and memory device, abstract).

Claim 2 is rejected using the same rationale as for the rejection of claim 1 above.

Claim 5 is rejected using the same rationales as for the rejections of claims 1-2 above.

For claim 6, Iwamura discloses the plurality of memory arrays that are divided into the plurality of banks support pipeline access to a plurality of data pipes that interface with the plurality of memory arrays (signal transmission lines connecting microprocessors are assigned to buses connected to repeaters including pipeline latches... each repeater for controlling the signal transmission between microprocessors is one of a data processing device, a memory device, and a functional device including bus switch means having a pipeline latch, col. 4, lines 33-46; microprocessors incorporate a signal transmission line for each transmission stage interconnecting functional blocks, col. 4, lines 12-14).

For claim 7, Iwamura discloses at least one data pipe is used for a reading operation (signal transmission lines corresponding to signal transmission stages, between an address input circuit to a read data output circuit, col. 4, lines 51-53).

For claim 8, Iwamura discloses at least one data pipe is used for a writing operation (signal transmission lines corresponding to signal transmission stages, arep

rovided between a write control signal input circuit and a write control circuit and between a write data input circuit and the write control circuit, col. 4, lines 55-59).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwamura et al (US Patent No. 6,467,004) and Rao (US Patent No. 6,173,356).

For claim 3, Iwamura discloses the invention as per the rejection of claim 1 above. Iwamura does not, however, expressly disclose the apparatus architecture coupled to the plurality of memory arrays is a non-pipelined microprocessor architecture.

Rao, however, discloses a memory system having a memory controller for linking a plurality of processors with an integrated memory, which comprises a plurality of state random access arrays (abstract).

Rao and Iwamura are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a non-pipelined microprocessor architecture to be coupled to a plurality of memory arrays

because this allows for efficient accessing of blocks of data as required by a multiple CPU data processing system (col. 2, line 67; col. 3, line1), as taught by Rao.

7. Claims 4 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwamura et al (US Patent No. 6,467,004) and Witt et al (US Patent No. 5,867,683).

For claim 4, Iwamura discloses the invention as per the rejection of claim 2 above. Iwamura does not, however, expressly disclose the pipelined processor supports out-of-order data processing operations and the plurality of memory arrays supports out-of-order data processing operations.

Witt, however, discloses instructions are dispatched in program order, issued and completed out of order, and retired in order (col. 9, lines 19-20).

Witt and Iwamura are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include out-of-order data procession operations and support thereof because this permits achievement of high performance (col. 9, lines 21-22), as taught by Witt.

For claim 14, Iwamura discloses the invention as per the rejection of claim 6 above. Iwamura does not, however, disclose the pipelined memory array is divided into a horizontal arrangement.

Witt, however, discloses stages of a microprocessor pipeline are listed horizontally at the top of timing diagrams (col. 32, lines 32-33).

Witt and Iwamura are analogous art in that they are of the same field of endeavor, that is, a memory device and the control thereof. It would have been obvious to a person of ordinary skill in the art at the time of the invention to divide the pipelined memory array into horizontal and vertical arrangements because this would illustrate the status of selected signals in a microprocessor throughout the multiple stages of the pipeline thereof (col. 32, lines 19-21), as taught by Witt.

For claim 15, Iwamura discloses the invention as per the rejection of claim 6 above. Iwamura does not, however, disclose the pipelined memory array is divided into a vertical arrangement.

Witt, however, discloses signals which composes timing diagrams are listed vertically at the left of the diagrams (col. 32, lines 33-35).

Witt and Iwamura are analogous art in that they are of the same field of endeavor, that is, a memory device and the control thereof. It would have been obvious to a person of ordinary skill in the art at the time of the invention to divide the pipelined memory array into horizontal and vertical arrangements because this would illustrate the status of selected signals in a microprocessor throughout the multiple stages of the pipeline thereof (col. 32, lines 19-21), as taught by Witt.

8. Claims 9 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwamura et al (US Patent No. 6,467,004) and Potter (US Patent No. 6,505,269).

For claim 9, Iwamura discloses the invention as per the rejection of claim 6 above. Iwamura does not, however, expressly disclose there are at least eight banks in each array.

Potter, however, discloses there are preferably eight independent banks of memory available to the processors (col. 7, lines 41-43).

Potter and Iwamura are analogous art in that they are of the same field of endeavor, that is, a memory device and the control thereof. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include at least eight banks in each array because this arrangement is significant to a streaming mode of operation wherein interleaving occurs between the banks and the arrays (col. 7, lines 43-45), as taught by Potter.

For claim 18, Iwamura discloses the invention as per the rejection of claim 6 above. Iwamura does not, however, expressly disclose memory operations from different banks having different memory addresses are interleaved.

Potter, however, discloses interleaving occurs between banks and arrays of memory (col. 7, line 45).

Potter and Iwamura are analogous art in that they are of the same field of endeavor, that is, a memory device and the control thereof. It would have been obvious to a person of ordinary skill in the art at the time of the invention to allow different memory addresses to be interleaved because this arrangement contributes to a streaming mode of operation (col. 7, lines 43-45), as taught by Potter.

9. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwamura et al (US Patent No. 6,467,004), and Martin et al (US PGPub No. 20020156995).

For claim 10, Iwamura discloses the invention as per the rejection of claim 6 above. Iwamura does not, however, expressly disclose a number of pipeline stages used depends upon an access latency of each bank and a desired throughput rate.

Martin, however, discloses the optimal number of stages for maximum throughput is determined by the ratio of the cycle period over the forward latency of a pipeline stage.

Martin and Iwamura are analogous art in that they are of the same field of endeavor, that is, a memory device and the control thereof. It would have been obvious to a person of ordinary skill in the art at the time of the invention that a number of pipeline stages used depends upon an access latency of each bank and a desired throughput rate because, when fine pipelines are desirable, the number of pipeline stages may be changed in order to achieve desired high-throughput and low latency (par. 0096), as taught by Martin.

10. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwamura et al (US Patent No. 6,467,004) and Tsuruta et al (US PGPub No. 20030037226).

For claim 11, Iwamura discloses the invention as per the rejection of claim 6 above. Iwamura does not, however, expressly disclose a clock frequency and a data path width for the pipeline is determined.

Tsuruta, however, discloses a processor architecture comprising a pipeline, shared by each of the program streams, having N pipeline stages operable at a frequency F, an instruction developing section which develops one instruction into Q parallel instructions, and a first mechanism executing one program stream for every M cycles depending on a required operation performance and selectively executing the Q parallel instructions (par. 0018).

Tsuruta and Iwamura are analogous art in that they are of the same field of endeavor, that is, a memory device and the control thereof. It would have been obvious to a person of ordinary skill in the art at the time of the invention that a clock frequency and data path width for a pipeline may be determined because this would allow for the system to suit a required performance and further reduce power consumption (par. 0018), as taught by Tsuruta.

11. Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwamura et al (US Patent No. 6,467,004) and Zahir et al (US Patent No. 6,052,802).

For claim 12, Iwamura discloses the invention as per the rejection of claim 6 above. Iwamura does not, however, disclose a number of pipeline stages is related to a number of clock cycles.

Zahir, however, discloses a number of computer cycles equal to the number of pipeline stages contained in a computer (col. 1, lines 26-27).

Zahir and Iwamura are analogous art in that they are of the same field of endeavor, that is, a system and method for memory control. It would have been obvious

to a person of ordinary skill in the art at the time of the invention to make a number of pipeline stages related to a number of clock cycles because it is common knowledge that a design technique called a pipeline involves the output of one process to serve as input to a second, etc., during which one or more processes occur during a computer clock cycle (col. 1, lines 13-20), as taught by Zahir.

Claim 13 is rejected using the same rationale as for the rejection of claim 12 above.

12. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwamura et al (US Patent No. 6,467,004) and Won et al (US Patent No. 6,498,764).

For claim 16, Iwamura discloses the invention as per the rejection of claim 6 above. Iwamura does not, however, disclose a writing operation into memory is performed by pumping an address with data that is to be written into memory.

Won, however, discloses a selecting means for enabling one of the plurality of the banks depending on the bank address allocated to the input address and the write address to perform the write operation and a pumping means for supplying a given bias to the bank (col. 2, lines 30-36).

Won and Iwamura are analogous art in that they are of the same field of endeavor, that is, a system and method for memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to pump an address with data that is to be written into memory because this would supply a given bias to the bank as need be (col. 2, lines 35-36), as taught by Won.

13. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwamura et al (US Patent No. 6,467,004), Witt et al (US Patent No. 5,867,683), and Iino et al (US Patent No. 5,586,282).

For claim 17, the combined teachings of Iwamura and Witt disclose the invention as per the rejection of claims 6 and 15 above. Iwamura and Witt do not, however, disclose allowing the address to flow through an address pipe to reach individual banks one cycle at a time.

Iino, however, discloses a microprocessor using one cycle of one or two clocks, (abstract), wherein the microprocessor generates an address data to execute an operation by outputting the data corresponding to the address data on a data bus in a write cycle... the microprocessor can be informed of the bank number from an external source and is provided with a signal terminal for information of the bank number (col. 9, lines 15-23).

Iino, Iwamura and Witt are analogous art in that they are of the same field of endeavor, that is, a system and method for memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to allow the address to flow through an address pipe to reach banks one cycle at a time because this allows for easy indication of completion of data access for a bank, for higher speed data accesses (abstract).

14. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwamura et al (US Patent No. 6,467,004), Makuta et al (US PGPub No. 20020186589), and the applicant's own admitted prior art (hereafter referred to as APA).

For claim 19, Iwamura discloses the invention as per the rejection of claim 6 above. Iwamura does not, however, disclose all peripheral access is accomplished from one side of a systolic memory array.

The concept of a systolic memory array is described in APA under the applicant's background section. Further, Makuta discloses a peripheral circuit along one side of a memory array (col. 15, lines 65-67; fig. 7, item 50).

Makuta, Iwamura and APA are analogous art in that they are of the same field of endeavor, that is, a system and method for memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to allow all peripheral access to be accomplished from one side of a memory array because as a design choice, this would make a more organized layout allowing for easy peripheral connection (fig. 7, item 50), as taught by Makuta.

15. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwamura et al (US Patent No. 6,467,004) and Jeddeloh (US PGPub No. 20040199739).

For claim 20, Iwamura discloses the invention as per the rejection of claim 6 above. Iwamura does not, however, disclose whenever a bank receives a read address, memory access is initiated.

Jeddeloh, however, discloses a memory address module starts sending the address for a first memory request to the memory module. The memory address module asserts the row address strobe and sends the row address to the memory module across an address line (par. 0041).

Jeddeloh and Iwamura are analogous art in that they are of the same field of endeavor, that is, a system and method for memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to initiate memory access whenever a bank receives a read address because this is a common process performed by a memory controller for such requests (par. 0040), as taught by Jeddeloh.

16. Claims 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Berg et al (US Patent No. 6,732,247) and the applicant's own admitted prior art (hereafter referred to as APA).

For claim 25, Berg discloses a processing system comprising: a die including a microprocessor (a processor die serving as an addressable on-chip memory, col. 1, line 67; col. 2, line 1); peripheral equipment coupled to the processing system (the computing system also includes a display, one or more input devices, one or more peripheral devices, col. 3, lines 23-31); communication channels and paths (data is moved between main memory of the computing system and the processor via a bus among one or more system buses, col. 3, lines 21-23); a network interface (computing system with pipelined data banks may include a communication or network interface, col. 3, lines 32-34); and on-die and off-die storage media wherein said storage media is

a memory array (a multi-ported pipelined memory that is located on a processor die serving as an addressable on-chip memory, col. 1, lines 66-67, col. 2, line 1).

Berg does not, however, expressly disclose said memory array is a systolic memory array. For this concept, the APA background section discloses systolic memory arrays for mapping computations or processes into memory structures.

Berg and APA are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include systolic memory arrays for said storage media because systolic memorys are easier to implement because of their modular designs and they are also more cost effective to produce because of this modular characteristic (APA background, par. 6).

Claim 26 is rejected using the same rationales as for the rejections of claims 5 and 25 above.

Allowable Subject Matter

17. The following is an examiner's statement of reasons for indicating allowable subject matter:

For claim 21, no combination of the aforementioned references describe access latency for a bank is represented by 2i+L, where i represents the time it takes to allow an address to reach a desired i th bank and L represents the cycles of latency to access the memory.

Claims 22-24 are allowable as being, directly or indirectly, dependent on claim 21 and having additional allowable features therein.

Citation of Pertinent Prior Art

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Gillingham (US Patent No. 6,546,476) discloses a method and apparatus for optimizing the efficiency of a data bus for a memory device in which extra latency is added between the time a memory controller issues a write instruction and the time the data is transferred on the data bus, to reduce the number of idle time slots on the data bus when switching between a read instruction and a write instruction.

Nowshadi (US PGPub No. 20040076044) discloses a technique for improving access latency of multiple bank DRAMs, in which address lines may be swapped to improve DRAM access latency and performance.

Contact Information

19. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 8:30am-5pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan, is also reachable at 571-272-4210.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information from

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. All questions regarding access to the Private PAIR system should be directed to the Electronic Business Center (EBC), reachable at 866-217-9197.

DK

1-23-06

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